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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,464	04/20/2001	Jeffrey M. Mason	X-658 US	2465

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EXAMINER	
OWENS, DOUGLAS W	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/839,464	Applicant(s) MASON ET AL.	
	Examiner Douglas W Owens	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) *72-75* is/are withdrawn from consideration.

5)☒ Claim(s) *69-71* is/are allowed.

6)☒ Claim(s) *1,5,8,9,11,13,14,23-26,29,33,35,37-43 and 76-79* is/are rejected.

7)☒ Claim(s) *2-4,6,7,10,12,15-22,27,28,30-32,34,36 and 44-68* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *20 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of the invention of group I, claims 1 – 71 and 76 – 79 in Paper No. 5 is acknowledged.

Claim Objections

2. Claims 12, 37 and 47 are objected to because of the following informalities:

Claims 12 and 47recite the limitation, "...EDIF..." without defining what an EDIF file is, or what the letters of the acronym mean.

Claim 37 recites the limitation, "...at least one module another time..." in lines 2 and 3. Should "another" be replaced with "at a" or some other phrase? There is no prior reference of time with respect to the floorplanning step.

In line 2 of claim 37, "necessitates" should be replaced with, "comprises", "includes" or similar legal terminology.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5, 11, 13, 14, 24, 26, 29, 33, 35, 37 – 41 are rejected under 35 U.S.C. 102(b) as being anticipated by US patent No. 5,870,308 to Dangelo et al.

Regarding claim 1, Dangelo et al. teaches a method for providing modular design in a programmable logic device (Col. 48, lines 45 – 50), the method comprising:

partitioning a top-level logic design into a plurality of modules (Col. 4, lines 11 – 14);

implementing each module using information generated by the partitioning step (Col. 4, lines 24 – 32; Col. 4, lines 44 – 47); and

assembling the modules using the information generated from the implementing step and the partitioning step (Col. 4, lines 24 – 26; Col. 6, lines 37 – 39; Col. 10, lines 11 – 16).

Regarding claim 5, Dangelo et al. teaches a method, wherein the step of partitioning includes sizing and positioning each module on the programmable logic device (Col. 4, lines 12 – 13; Col. 4, lines 45 – 47; Col. 14, lines 20 – 31).

Regarding claim 11, Dangelo et al. teaches a method, wherein the step of partitioning includes generating a first file comprising a description of a top-level logic design in primitive elements (Col. 4, lines 11 – 21).

Regarding claim 13, Dangelo et al. teaches a method, wherein the step of partitioning includes generating a second file comprising inter-module timing constraints for the top-level logic design (Col. 4, lines 57 – 62).

Regarding claim 14, Dangelo et al. teaches a method, wherein the second file comprises a top-level netlist constraints file (Col. 4, lines 32 – 35).

Regarding claim 24, Dangelo et al. teaches a method, wherein the implementation of the plurality of modules is performed. Dangelo et al. is silent with

respect to the order that the plurality of modules is implanted. However, since the plurality of modules are implemented, they must be implemented in some order. Therefore, the limitation of "any order" is met by Dangelo et al., since "any order" does not require a particular order of implementation, any order will do.

Regarding claim 26, Dangelo et al. teaches a method, wherein the top-level logic design provides context for the module implementation.

Regarding claim 29, Dangelo et al. teaches a method, wherein the step of implementing includes mapping each module.

Regarding claim 33, Dangelo et al. teaches a method, wherein the step of implementing includes placing and routing each module.

Regarding claim 35, Dangelo et al. teaches a method, wherein the step of implementing includes floorplanning at least one module (Col. 14, lines 19 – 31).

Regarding claim 37, Dangelo et al. teaches a method, wherein floorplanning comprises mapping, placing, and routing at least one module.

Regarding claim 38, Dangelo et al. teaches a method, wherein the step of implementing includes simulating each module (Col. 6, lines 37 – 39).

Regarding claim 39, Dangelo et al. teaches a method, wherein simulating is performed using the top-level logic design as context.

Regarding claim 40, Dangelo et al. teaches a method, wherein simulating is performed independently from the top-level logic design.

Regarding claim 41, Dangelo et al. does not explicitly teach simulating dangling signals of the module. Dangelo et al. teaches simulating the module and the assembled device. This simulation would have inherently included dangling signals.

5. Claim 76 is rejected under 35 U.S.C. 102(b) as being anticipated by US patent No. 4,646,266 to Ovshinsky et al.

Ovshinsky et al. teaches a programmable logic device, including logic implemented by configuration data (Col. 1, lines 12 – 68, for example).

Ovshinsky et al. does not teach a programmable logic device, wherein the configuration data is generated as recited in claim 76 of the instant application. These are considered product-by-process limitations. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

6. Claims 78 and 79 are rejected under 35 U.S.C. 102(b) as being anticipated by US patent No. 5,309,371 to Shikata et al.

Regarding claim 78, Shikata et al. teaches a method of positioning modules of a programmable logic design (Col. 1, lines 8 – 18) comprising:

representing elements and connection of the design on a computer monitor (Col. 1, lines 34 – 50; Figs. 9 – 11, for example);

drawing a boundary around elements of the design;

drawing a second boundary around a second group of elements; and

repeating until all elements are enclosed.

Regarding claim 79, Shikata et al. teaches a method of positioning modules, wherein the boundaries are rectangular.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8, 9 25, 42, 43 and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo et al.

Regarding claims 8, 9, 25 and 43, Dangelo et al. does not explicitly teach a method, wherein the step of partitioning includes creating a physically implemented module directory. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make a physically implemented module directory, since it is desirable to maintain organization and order throughout the design process.

Regarding claim 42, Dangelo et al. does not teach a method, wherein the step of implementing includes publishing predetermined files for each module to a centralized directory. It would have been obvious to one of ordinary skill in the art at the time the invention was made to publish predetermined files for each module to a centralized directory, since it is desirable for design engineers to have access to the modules.

Regarding claim 77, Dangelo et al. teaches a method for providing a modular design in a programmable logic device, the method comprising:

partitioning a top-level logic design; and

implementing the modules.

Dangelo et al. does not teach a plurality of ports for connecting the modules or where critical paths in the design are inside a module. It would have been obvious to one of ordinary skill to include a plurality of ports for connecting the modules, since it is intended for the modules to be connected and simulated together before reduction to practice. It would have also been obvious to have the critical paths inside a module since they are a critical part of the device and must also be simulated for testing device function and verifying timing.

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo et al. as applied to claim 1 above, and further in view of US patent No. 6,446,243 to Huang et al.

Dangelo et al. does not teach a method, wherein the implementation of at least two modules is performed in parallel. Huang et al. teaches a method of modular design method, wherein the implementation of at least two modules is performed in parallel (Col. 4, lines 23 – 28). It would have been obvious to one of ordinary skill in the art to incorporate the method taught by Huang et al. into the method taught by Dangelo et al., since it is desirable to produce complete designs quickly and accurately.

Allowable Subject Matter

10. Claims 69 – 71 are allowed.

11. Claims 2 – 4, 6, 7, 10, 15 – 22, 27, 28, 30 – 32, 34, 36, 44 – 46 and 48 – 68 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DWO

TOM THOMAS
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